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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/439,061	11/12/1999	ROBERT J. PROEBSTING	939A-350-1-2	1190

20350 7590 05/21/2003

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EXAMINER

YENKE, BRIAN P

ART UNIT

PAPER NUMBER

2614

DATE MAILED: 05/21/2003

12

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

09/439,061

Applicant(s)

PROEBSTING, ROBERT J.

Examiner

BRIAN P. YENKE

Art Unit

2614

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 18 December 2002.
- 2a) ☒ This action is FINAL.                      2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 20-25 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 20-25 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on \_\_\_\_\_ is: a) ☐ approved b) ☐ disapproved by the Examiner.  
If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a) ☐ All b) ☐ Some \* c) ☐ None of:  
1. ☐ Certified copies of the priority documents have been received.  
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).  
\* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).  
a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) \_\_\_\_\_
- 4) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_

### DETAILED ACTION

1. Applicant's request for reconsideration of the finality of the rejection of the last Office action is persuasive and, therefore, the finality of that action is withdrawn.
2. The applicant stated that the Article "An Embedded Frame Buffer for Graphics Applications" attached as Appendix A in the disclosure, was never published. The examiner has attached the IEEE papers to the office action (PTO-892), which shows that the article was indeed published 19 Dec 1996. Since the applicant's effective filing date is 09 ~~Nov~~<sup>Aug</sup> 96 and the article was published subsequently, the examiner has removed the Article in the rejection. Thus in this rejection, the examiner is maintaining the grounds of the rejection set forth (05 July 2002/Paper 7) and thus this action is being made final.
3. Applicant's arguments filed 15 October 2002 have been fully considered but they are not persuasive.

### ***Claim Rejections - 35 USC § 103***

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 20-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over May, US 5,815,168.

In considering claims 20-23,

- 1) the claimed segmenting a plurality of pixels... is met controller 510 which is coupled to host CPU 540, and transfers data to display memory 550 via memory controller 520, where the pixels may be ordered within a row of memory in a scan-line format (left to right, top to bottom) or in another format are stored in a tiled address format
- 2) the claimed storing data representing each of said plurality of pixel groups is met by display memory 550 which stores the tiled pixels.

However, May remains silent on the storing data in non-adjoining arrays.

May discloses a "Tiled Memory Addressing With Programmable Tile Dimensions" where the tile shape and dimensions are optimized for sizes and shapes of blocks of pixel data to be transferred to the display memory (col 4, line 53-56). The tile dimensions which include tile size and tile height are programmable parameters stored in software (col 6, line 20-30). The parameters may also be determined by software depending upon video mode, resolution, and pixel depth. As defined by May, tile size(aspect ratio) is the number of pixels in a tile which is the same as the number of pixels which may fit into one row of the DRAM array. Also, May discloses that subsequent accesses to data words in different columns of the same row (column accesses) are much faster than accesses to different rows. May discloses depending upon the graphics or video image to be displayed a sequential scan-line based addressing scheme may create a bottleneck when data is input into the memory (col 2, line 28-41).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention, to modify May, which discloses a system which optimizes tile shape and dimensions for pixel data to be in stored in memory based upon the video mode, resolution and pixel depth, by storing data in either an odd or even array when a received signal (video mode) comprises odd and even lines, which would provide faster access time and prevent bottlenecking from occurring.

In considering claims 24-25,

May does not specifically disclose, dividing the display panel into a first half and a second half. May discloses a system where a depending upon the application type, a particular tile size (i.e. aspect ratio) may provide optimal performance depending upon the type of data being transferred. Where transfers of text data may perform optimally with long, narrow tiles for text and graphical images and video on the other hand may be optimized using taller more rectangular or square tile shapes.

Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to modify May which discloses a system which divides the pixel data into an appropriate tile shape/size based upon the type of video mode, resolution, pixel depth of the signal, by dividing the display into respective portions based on the users needs and the type of signal to be displayed.

For Motivation/Comments regarding arrays, refer to claim 20 rejection above.

***Applicant's Arguments***

- a) Regarding claim 20, applicant states that May does not disclose storing the data in non-adjoining arrays.
- b) Regarding claim 25, applicant states that May does not disclose using non-adjoining arrays, not using odd numbered arrays for a first half of the pixels and even numbered arrays for a second half of pixels.

***Examiner's Response***

- a) The examiner agrees. However, the examiner maintains this limitation would have been an obvious modification to May's system as described above/repeated below.

May discloses a "Tiled Memory Addressing With Programmable Tile Dimensions" where the tile shape and dimensions are optimized for sizes and shapes of blocks of pixel data to be transferred to the display memory (col 4, line 53-56). The tile dimensions which include tile size and tile height are programmable parameters stored in software (col 6, line 20-30). The parameters may also be determined by software depending upon video mode, resolution, and pixel depth. As defined by May, tile size(aspect ratio) is the number of pixels in a tile which is the same as the number of pixels which may fit into one row of the DRAM array. Also, May discloses that subsequent accesses to data words in different columns of the same row (column accesses) are much faster than accesses to different rows. May discloses depending upon the graphics or video

image to be displayed a sequential scan-line based addressing scheme may create a bottleneck when data is input into the memory (col 2, line 28-41).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention, to modify May, which discloses a system which optimizes tile shape and dimensions for pixel data to be in stored in memory based upon the video mode, resolution and pixel depth, by storing data in either an odd or even array when a received signal (video mode) comprises odd and even lines, which would provide faster access time and prevent bottlenecking from occurring.

b) The examiner agrees. However, the examiner maintains this would have been an obvious modification to May's system as stated above/repeated below.

May discloses a system where a depending upon the application type, a particular tile size (i.e. aspect ratio) may provide optimal performance depending upon the type of data being transferred. Where transfers of text data may perform optimally with long, narrow tiles for text and graphical images and video on the other hand may be optimized using taller more rectangular or square tile shapes.

Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to modify May which discloses a system which divides the pixel data into an appropriate tile shape/size based upon the type of video mode, resolution, pixel depth of the signal, by dividing the display into respective portions based on the users needs and the type of signal to be displayed.

***Conclusion***

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Lim, US 5,291,443 discloses a memory array configuration of memory cells that allows simultaneous read and refresh of the memory cells.

Buckelew et al., US 5,864,512 discloses a "High Speed Video Frame Buffer Using Single Port Memory Chips" where the buffer memory is subdivided into a plurality of blocks, each block corresponding to a region of the display.

Lu et al., US 5,781,200 (previously cited), discloses a tile memory mapping which utilizes the fact that a single row of sense amplifiers per array, so rows of the same array conflict since they cannot be open at the same time. (It is noted by the examiner, the filing date of Lu (08 Aug 96) is one day prior to the applicant's effective filing date (09 Aug 96).

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of



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the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian Yenke whose telephone number is (703) 305-9871. The examiner work schedule is Monday-Thursday, 0730-1830 hrs.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's Supervisor, John W. Miller, can be reached at (703)305-4795.

**Any response to this action should be mailed to:**

Commissioner of Patents and Trademarks

Washington, D.C. 20231


**or faxed to:**

**(703) 872-9314**

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth Floor (Receptionist). Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 305-4700.

B.P.Y.

09 May 2003

  
**JOHN MILLER**  
**SUPERVISORY PATENT EXAMINER**  
**TECHNOLOGY CENTER 2600**